AMENDMENTS TO THE SPECIFICATION

(Paragraph numbers from the Publication of March 21, 2002)

[0059] The standard fibre channel address format for the FICON D_ID is shown at the top of FIG. 5A and includes three 8 bit address fields in the 24 bit address: domain (D), port (P) and loop (L). The non-standard, internal switch element format for the internal D_ID is shown at the bottom of FIG. ~~5B~~ 5A and includes 4 bit fabric (F) field, 6 bit chassis (C) field, 2 bit switch (S) field, 2 bit port (P) field, ~~6~~ 8 bit loop (L) field. Mapping typically occurs for all Domain Addresses except Domain IDs of F0h-FFh.

[0088] The Primitive Insert Logic (PIL) consists of the Primitive MUX 446 and the Primitive Memory & Generator logic ~~448~~ 444. When the IFP detects a primitive, it activates one of the 5 PRIMITIVE lines to the bypass mux. The PIL remembers the primitive that was detected. If the R_RDY count is non zero an R_RDY will be inserted to the switch element at the next opportunity (between SOF and EOF). If an OLS, NOS, LR, or LRR is detected, a bit is set to remember its reception and the sequence is inserted to the switch element at the next opportunity. An R_RDY must be preceded and succeeded by 2 IDLE characters. Other Primitive Sequences require at least 3 repetitions of the Primitive to be valid. The PIL generates these sequences whenever primitives are inserted. The INSERTING signal is used to select the Primitive Signal or Primitive Sequence to the output of the Primitive Mux 446 and is also passed to the FIFO controller to inhibit FIFO output during this time.

[0095] Referring now to FIG. 12, operation of the data buffer extension feature of the present system is illustrated. Only those elements introduced in the foregoing description that are needed for describing the feature are shown. As described above, the FPGA 400 includes a FIFO controller 410 and an R_RDY detector 414. Also shown are inbound frame SOF detector 420A, bypass frame SOF detector 442A, bypass frame EOF detector 442B, inbound frame counter 434A and FIFO counter 434B. The FPGA is shown connected to one of the FIFOs 402, though it should be understood from the foregoing description that additional FIFOs can be included. An output of the FPGA is also connected to a buffer 310A of the switch element 310. As indicated, the buffer ~~434A~~ 310A holds up to 8 frames and the FIFO 402 holds up to 58 frames. Multiplexer 411

selects between an inbound frame and a line connected to a read data line from the FIFO 402.